

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANT : **HUBER, LOUIS P., et al.**  
SERIAL NO : Divisional of U. S. Serial No. 09/811,844 filed 3/19/2001  
TITLE : POWER CHIP RESISTOR  
  
Grp./A.U. : 2832  
Examiner : Easthom, Karl D.  
Conf. No. :  
Docket No. : P04870US1

**PRELIMINARY AMENDMENT FOR DIVISIONAL APPLICATION**

Assistant Director for Patents  
Washington, D.C. 20231

Dear Sir:

Please preliminarily amend the above-entitled application as follows:

**In the Title**

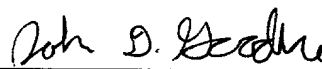
Please amend the title to: METHOD FOR MANUFACTURING A POWER CHIP  
RESISTOR.

**In The Specification**

Please add the following as the first paragraph of the Specification:

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**CERTIFICATE OF MAILING (37 C.F.R. § 1.8(a))**

I hereby certify that this document and the documents referred to as enclosed therein are being deposited with the United States Postal Service as Express mail in an envelope addressed to: Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231, on this 6<sup>th</sup> day of March, 2002.

  
John D. Goodhue

## PRIORITY STATEMENT

This application is a Divisional of U. S. Patent Application Serial No. 09/811,844 filed on March 19, 2001.

### In The Abstract

Please replace the Abstract with the following:

The invention provides for a method of manufacturing a stacked power chip resistor. The method includes adhering a first chip resistor to a second chip resistor with a glass encapsulant, connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor with the first metal barrier, and connecting a second terminal on the first chip resistor to a second terminal of the second chip resistor with a second metal barrier.

### In the Claims

Please cancel claims 1-25 without prejudice.

Please amend claim 26 as follows:

#### 26. (Amended)

A method of manufacturing a stacked power chip resistor comprising:  
adhering a first chip resistor to a second chip resistor with a glass encapsulant;  
connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor with a first metal barrier;  
connecting a second terminal of the first chip resistor to a second terminal of the second chip resistor with a second metal barrier.

Kindly enter the following new claims 29-32:

29. The method of claim 26 further comprising of adhering a third chip resistor to the second chip resistor with a second glass encapsulant.

30. The method of claim 26 wherein the glass encapsulant is glass frit.

31. The method of claim 26 wherein the first chip resistor and the second chip resistor are thick film resistors.

32. A method of manufacturing a stacked power chip resistor comprising:  
adhering with a glass encapsulant a first chip resistor having a first substrate and a first resistive element to a second chip resistor having a second substrate and a second resistive element;  
connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor with a first metal barrier; and  
connecting a second terminal of the first chip resistor to a second terminal of the second chip resistor with a second metal barrier.

## REMARKS

The Applicant has filed this divisional to pursue that species not elected in the parent application. Thus, the Applicant cancels claims 1-25. Claims 26-32 are pending. Claims 29-32 are new.

In addition, the Title and the Abstract have been amended to reflect the species being pursued, and the proper priority statement has been added. The Abstract does not add new matter and is consistent with claim 26.

### NEW CLAIMS

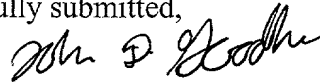
Applicant has amended the application to add new claims 29-32. Support for the new claims should be apparent from the application as originally filed, particularly the original claims and Figures 1-4.

Favorable action is respectfully requested. No fees or extensions of time are believed to be due in connection with this Preliminary Amendment; however, this paper should be considered such a request if necessary, and any deficiency in fees should be charged to Deposit Account No. 26-0084.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Examiner is respectfully urged to call the undersigned attorney at (515) 288-3667 to discuss the claims in an effort to reach a mutual agreement with respect to claim limitation in the present application if the Examiner does not find that all present claims should be allowed.

Respectfully submitted,



JOHN D. ~~GOODHUE~~, Reg. No. 47,603  
McKEE, VOORHEES & SEASE, P.L.C.  
801 Grand Avenue, Suite 3200  
Des Moines, Iowa 50309-2721  
Phone No. (515) 288-3667  
Fax No. (515) 288-1338  
**CUSTOMER NO: 22885**

Attorneys of Record

- bja -

Application No. P04870US1

**AMENDMENT — VERSION WITH MARKINGS  
TO SHOW CHANGES MADE**

**In the Title**

Please amend the title to:

METHOD FOR MANUFACTURING A POWER CHIP RESISTOR

**In The Specification**

Please add the following as the first paragraph of the Specification:

**PRIORITY STATEMENT**

This application is a Divisional of U. S. Patent Application Serial No. 09/811,844 filed on  
March 19, 2001.

**In The Abstract**

~~A method and apparatus for a stacked power chip is disclosed. The invention provides for multiple power chip resistors to be stacked, providing for encapsulant such as glass to separate each power chip resistor and a metal barrier such as nickel plating on each end of the stacked power chip resistor to provide for electrical and mechanical connection of each power chip resistor in the stack.~~

The invention provides for a method of manufacturing a stacked power chip resistor. The method includes adhering a first chip resistor to a second chip resistor with a glass encapsulant, connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor

with the first metal barrier, and connecting a second terminal on the first chip resistor to a second terminal of the second chip resistor with a second metal barrier.

**In the Claims**

Please cancel claims 1-25 without prejudice.

Please amend claim 26 as follows:

26. (Amended)

A method of manufacturing a stacked power chip resistor comprising:  
adhering a first chip resistor to a second chip resistor with a glass encapsulant;  
connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor  
with a first metal barrier;  
connecting a second terminal of the first chip resistor to a second terminal of the second chip  
resistor with a second metal barrier.

Kindly enter the following new claims 29-32:

29. The method of claim 26 further comprising of adhering a third chip resistor to the second chip resistor with a second glass encapsulant.

30. The method of claim 26 wherein the glass encapsulant is glass frit.

31. The method of claim 26 wherein the first chip resistor and the second chip resistor are thick film resistors.

32. A method of manufacturing a stacked power chip resistor comprising:

adhering with a glass encapsulant a first chip resistor having a first substrate and a first resistive

element to a second chip resistor having a second substrate and a second resistive

element;

connecting a first terminal of the first chip resistor to a first terminal of the second chip resistor

with a first metal barrier; and

connecting a second terminal of the first chip resistor to a second terminal of the second chip

resistor with a second metal barrier.